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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/848,625	Applicant(s) HENRY ET AL.	
	Examiner Terry L Englund	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *18 October 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

The amendment and RCE submitted on May 14, 2003 were reviewed and considered with the following results:

The RCE was accepted and entered. Therefore, the amendment was also entered.

The objections to the drawings and disclosure, as described in the previous Office Action, have now been withdrawn. The comments described on pages 5-10 of the amendment were considered persuasive.

Amended claim 8 overcame the objections to claims 8-13, which have now been withdrawn.

The amended claims, and accompanying comments, overcame the rejections of claims 1-6, 8, 10-12, 17, and 18 under 35 U.S.C. 103(a) with respect to Tailliet. Those rejections have been withdrawn because Tailliet does not show the first and second signals providing power to the circuit as now recited, and understood, within each of independent claims 1, 8, 17, and 18. For example, although the signal Sd is provided to an input of circuit 3 (or 4), the circuit is considered to be actually powered by supply voltage Vdd.

The RCE provided additional time to consider the claimed limitations (previous and amended), reconsider prior art references, and perform a new, thorough search. When reconsidering claims 8-13, 17, and 18, and considering newly added claims 27-31, they were deemed to have limitations that require corrections and/or clarification. Those are described later under the appropriate section. Several recently found references, and one that had been previously cited, are deemed to read on the circuit powering limitations. Therefore, prior art

rejections are described later under the appropriate section. Also, when the limitations of claims 14-16 were reconsidered, it was determined at least one reference could also be considered as meeting them. Those rejections are also described later, and the previous Office Action's indication that claims 14-16 were allowable have been withdrawn. Also, the previous Office Action's indication that claims 7 and 20 were only objected to as being dependent upon a rejected base claim have been withdrawn in view of the new interpretations of the claimed limitations and prior art references considered.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-13, 17, 18 and 27-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The combination of the signal transfer, charge storage, and inverting circuits of claims 8 and 27 is misleading and/or inaccurate. As presently understood, the combination does not correspond to any of the applicants' own figures. For example, signal transfer circuit M1,M2 and charge storage circuit C1 of Fig. 7 provide the respective first and second signals to power circuit 710. However, inverting circuit M3,M4,C2, 540 does not receive either of those first and second signals. If M3,M4 are deemed the signal transfer circuit, and C2 is deemed the charge storage circuit, they do not provide signals that power (e.g. see the PWR pin) circuit 710. Therefore, clarification is requested with respect to what the applicants' limitations recited within claims 8 and 27 are intended to mean. The five separate means, "signal transfer circuit", and "charge storage circuit" recited within claim 18 are

confusing because they clearly overlap one another. For example, from the applicants' own Fig. 1, it appears Transient Rejecting Circuit 110 is the means for receiving and monitoring the supply signal, as well as determining normal and transient conditions, and for providing both the first and second signals. Although one of ordinary skill in the art would understand from the disclosure that the first signal is provided by the "Signal Transfer Circuit" means during normal operations, and the second signal is provided by the "Charge Storage Circuit" means when a transient occurs, what do the applicants refer to with respect to the receiving, monitoring, and determining means? Doesn't the signal transfer circuit means perform those functions, or are the various recited means meant to be specific, separate means? Therefore, clarification is requested (e.g. identify each means by pointing out in at least one of the applicants' figures what the various means correspond to). Similar to the various means and elements recited within claim 18, the various steps, and the "signal transfer circuit"/"charge storage circuit" recited within claim 17 are confusing. For example, do the applicants mean that separate elements perform each respective step, or do they also overlap?

Dependent claims carry over any rejection within a claim that they depend upon.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

In so far as being understood, claims 1-3, 5-7, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Holst et al. (Holst), a reference cited in a previous Office Action. Holst

shows an apparatus in Fig. 1 that effectively protects a circuit 101 from a transient event. The apparatus comprises a signal transfer circuit P1,N3,N2 that receives a supply signal IOVDD and outputs a first signal pllvdd, during normal operation, to a pin of circuit 101. This first signal charges charge storage circuit N4, wherein it is understood by one of ordinary skill in the art that circuit 101 is powered by the first signal during normal operation. Charge storage circuit N4 receives the first signal during normal operation, and stores enough charge to output a second signal (its stored voltage) to circuit 101's pin to power it during a transient event (e.g. see "temporal variations in the load of the circuit supplied by the PLLVDD supply" on column 5, lines 38-45). Therefore, one of ordinary skill in the art would understand that first signal pllvdd would be provided by signal transfer circuit P1,N3,N2 during normal operations, and a second signal (i.e. the stored charge) from charge storage circuit N4 is provided to power circuit 101 when the transient event occurs, anticipating claim 1. N4 will be effectively charged during normal operations, while discharging during a transient event that pulls pllvdd down temporarily, anticipating claim 2. P1,N2 of signal transfer circuit P1,N3,N2 can be deemed a transistor circuit that provides first signal pllvdd, anticipating claim 3. Since capacitor circuit N4 of charge storage circuit N4 receives and charges to first signal pllvdd during normal operations, and provides the second signal during the transient event, claims 5 and 6 are also anticipated. During normal operations, first signal pllvdd from first and second transistors P1,N2 prevent drain from charge storage circuit N4, thus anticipating claim 7. When the signal transfer circuit is providing the first signal, it can be deemed as configured to prevent the stored charge from charge storage circuit N4 from falling below a level required to power the circuit's pin, anticipating claim 19.

In so far as being understood, claims 1, 2, 4-6, and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Reasoner et al. (Reasoner), a reference found during a recent search. Fig. 1 shows an apparatus for protecting a circuit from a transient event (e.g. see the Abstract's "power fluctuations, power interruptions, and other short-duration power failures"). The apparatus comprises a signal transfer circuit 132 that receives a supply signal (e.g. 12V from 120) and output a first signal (e.g. 5V at node 130), during normal operation, to both a pin of the circuit 116 and to a charge storage circuit 112. Circuit 116 is powered by the first signal during normal operation. Charge storage circuit 112 receives the first signal during normal operation, and stores enough charge to output a second signal to circuit 116's pin to power it during a transient event (e.g. see column 5, lines 3-10 and 18-36). Therefore, claim 1 is anticipated. Since Reasoning discloses that charge storage circuit 112 charges when 120 provides power to circuit 116, and charge storage circuit 112 discharges when normal line power is lost or interrupted (e.g. see column 5, lines 3-10), one of ordinary skill in the art would understand the charging during normal operations, and the discharging during transient events, anticipating claim 2. With diodes 124 and 126 within signal transfer circuit 132, the diode circuit of claim 4 is anticipated. Charge storage circuit 112 comprises a capacitor, anticipating claim 5. Claim 6 is anticipated by the description on columns 4 (lines 41-52) and 5 (lines 3-10). Interpreting the figure in another manner, the upper lead of resistor 122 receives a supply signal from 120; and 132,112 monitor the supply signal for a transient event, and also determines when the circuit is in normal operation and when the transient event is occurring. For example, when 120 provides a sufficient voltage to keep the voltage at node 130 at 5 volts, the circuit is under normal operation. However, a transient event occurs when the node voltage drops below 5 volts

(e.g. see column 4, lines 50-58). During normal operation, first signal (e.g. 5V) from signal transfer circuit 132 is provided to a pin of circuit 116 to power it, and during a transient event, a second signal (the stored voltage) is provided from charge storage circuit 112 to power the pin of circuit 116, thus anticipating claim 17. The upper lead of resistor 122 is deemed a means for receiving a supply signal (from 120); 132,112 is a means for monitoring the supply signal to determine the transient event, and also a means for determining when circuit 116 is either in normal operation or when the transient event is occurring (as previously described); 132 is the means for providing first signal (e.g. 5V) from signal transfer circuit 132 to a pin of circuit 116 to power it, wherein 112 is the means for providing a second signal (e.g. stored voltage) to power circuit 116's pin when a transient event is occurring, anticipating claim 18. When the signal transfer circuit is providing the first signal, it can be deemed as configured to prevent the stored charge from charge storage circuit 112 from falling below a level required to power the circuit's pin, anticipating claim 19.

In so far as being understood, claims 1-7, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Konishi, another reference found during the recent search. Fig. 1 shows an apparatus comprising a signal transfer circuit 21-1,...,21-N,22 receiving supply signal VC1 and outputting a first signal VC2 during normal operation to both a pin of circuit 10 and to a charge storage circuit 23, wherein circuit 10 is powered by first signal VC2 during normal operation (e.g. see column 1, lines 45-47), and charge storage circuit 23 receives and charges to first signal VC2 during normal operation. During a transient event when a large consumption current is required, charge storage circuit 23 provides a second signal to help prevent instantaneous reduction of VC2 (e.g. see column 2, lines 20-30). Since VC2 is the operating voltage of circuit

10, one of ordinary skill in the art can deem the output of signal transfer circuit 21-1,...,21-N,22 as the first signal during normal operation, and the discharge of charge storage circuit 23 as the second signal during the large current consumption transient event, thus anticipating claims 1 and 2. Signal transfer circuit 21-1,...,21-N,22 comprises a transistor circuit 22 that provides the first signal VC2 during normal operation, anticipating claim 3. With diode configured transistors 21-1,...,21-N included in the signal transfer circuit, it can also be considered as comprising a diode circuit that helps to provide first signal VC2, anticipating claim 4. Charge storage circuit 23 comprises a capacitor circuit 23 that stores enough charge to provide the second signal during the transient event, wherein it charges to the first signal during normal operation, and discharges the second signal during the transient event. Therefore, claims 5 and 6 are anticipated. Since the signal transfer circuit comprises five transistors, it comprises first and second transistors. During normal operation, the transistors provide first signal VC2 to power circuit 10 and to charge charge storage circuit 23. At this time, when first signal VC2 is being provided, the transistors effectively prevent drain from charge storage circuit 23, anticipating claim 7. During normal operations, and at least part of the transient event, the signal transfer circuit prevents the stored charge from falling below a level required to power the circuit, thus anticipating claim 19.

Claims 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kirchhoff, a reference found during the recent search. Fig. 1 of Kirchhoff shows a complementary switch T1,T2 receiving an input signal IN and outputting an output signal E1,E2 to a pin (i.e. the common connection of E1,E2) of circuit I1,V1,FF; and a charge storage circuit T3 coupled to switch T1,T2 providing a secondary logic signal (e.g. the stored voltage) during a transient event. Although the reference does not clearly show or disclose input signal IN as a logic signal, one of

ordinary skill in the art would recognize the circuit is related to logic signals (i.e. input and output) due to flip-flop FF and its common input pin receiving E1,E2. The reference cites the circuit is used for noise signal suppression (e.g. see the Abstract and column 3, lines 30-31), and internal problems (e.g. in the supply voltage potential) is compensated for (e.g. see column 3, line 31 through column 4, line 5). Therefore, one of ordinary skill in the art would be able to relate these to transient events (e.g. noise within the input signal itself, and/or fluctuations of the supply voltage potential), wherein it is understood they refer to short, temporary changes. During normal operation, input signal IN passes through switch T1,T2 to circuit I1,V1,FF, as well as to charge storage circuit T3, wherein T3 will charge to the output logic signal during normal operation. If any transient events occurs (e.g. affecting either signal IN, or supply voltage potential VDD), the charge stored on charge storage circuit T3 can be deemed a secondary logic signal. This is because T3 will not have the time to charge or discharge in response to the transient, thus effectively maintaining a secondary logic signal that is equal to the stored voltage charge at E1,E2 during the transient event, helping protect the circuit I1,V1,FF from inadvertently changing logic states during the transient event, thus anticipating claims 14 and 15.

Due to the resistance of switch T1,T2's transistor circuit T1,T2, the switch will help prevent the drain of charge storage circuit T3 during a transient event, anticipating claim 16.

Claim Rejections under 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reasoner et al. (Reasoner) as applied to claim 1 above. As previously described, Reasoner shows and discloses an apparatus for protecting a circuit from a transient event. Although the reference does not clearly show or disclose the signal transfer circuit as comprising at least one transistor, Reasoner does disclose that "one skilled in the relevant art would find apparent" that signal transfer circuit 132 could "take on different configurations" (see column 4, lines 45-49). Since circuit 116 is disclosed as having CMOS RAM (e.g. see column 4, lines 23-23-27), it would have been obvious to one of ordinary skill in the art to use appropriately configured MOS type transistors to replace the resistor and diodes within charge storage circuit 132, rendering claims 3 and 7 obvious. The resistor and diode configured MOS transistors would provide the first signal 5V to circuit 116 during normal operations. A MOS transistor would take up less area than a resistor, and it would also provide a means to adjust the voltage drop between 120 and node 130 to obtain the proper, desired operational voltage with respect to the voltage available from 120. Since diode 124 already prevents drain from charge storage circuit 112 (e.g. see column 4, lines

54-58), the resistor and diode configured MOS transistors replacing resistor 122 and diode 124, respectively would also prevent drain from charge storage circuit 112. The use of MOS transistors within charge storage circuit 132 would make fabrication of Reasoner's circuit easier since all the elements would be similar in formation and could be made in the same process, and the transistors would also help ensure all the components within the overall circuit have similar operational characteristics (e.g. MOS transistors within circuit 116 and 132 would have similar temperature coefficients).

Claims 20-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holst et al. (Holst) as applied to independent claim 1 (and most of its dependent claims). [For example, claims 21, 22, and 24-27 closely correspond to claims 1, 2, and 5-7, respectively.] Since the signal transfer circuit, supply signal, first signal, normal operation, pin of a circuit, charge storage circuit, second signal, and transient event were already described previously with respect to the rejection of claim 1, those details will not be repeated here. However, independent claim 21 also recites the signal transfer circuit comprises a transistor circuit having a body connection coupled to the pin of the circuit, which is not clearly shown or disclosed by the reference of Holst. However, signal transfer circuit P1,N3,N2 does comprises transistor circuit P1,N2. The body connection of P1 is shown connected to 108, and even though the body connection of NMOS N2 is neither shown nor disclosed, it is believed its source is coupled to pin 110 of circuit 101 (e.g. the source of an NMOS transistor is typically coupled to the lower of the voltages applied to its source and drain). Therefore, it would have been obvious to one of ordinary skill in the art to also believe the body connection of transistor N2 is coupled to the circuit's pin, thus rendering claims 20 and 21 obvious. Unless a reference clearly indicates otherwise, with respect

to the body connection (e.g. bulk, body, or backgate) of a MOS transistor, it is typically connected to the transistor's source. In this case, the body connection of transistor N2 is considered connected to its source, which is connected to pin 110 of circuit 101. For the same reasoning as applied to closely related claims 2, and 5-7 described within the 35 U.S.C. 102(b) rejections, claims 22, and 24-26 are also rendered obvious. As long as P1,N3,N2 are providing first signal pllvdd, the signal transfer circuit can be deemed as being configured to prevent the stored charge of charge storage circuit N4 from falling below a level required to power pin 110 of circuit 101, rendering obvious claim 23

Claims 20-26 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Konishi, the reference found during the recent search, applied to independent claim 1 (and most of its dependent claims). [For example, claims 21, 22, and 24-27 closely correspond to claims 1, 2, and 5-7, respectively.] Since the signal transfer circuit, supply signal, first signal, normal operation, pin of a circuit, charge storage circuit, second signal, and transient event were already described previously with respect to the rejection of claim 1, those details will not be repeated here. However, independent claim 21 also recites the signal transfer circuit comprises a transistor circuit having a body connection coupled to the pin of the circuit, which is not clearly shown or disclosed by the reference of Konishi. However, signal transfer circuit 21-1,...,21-N,22 does comprises a transistor circuit 21-1,...,21-N,22. Although none of the transistors are shown with any type of body connection, NMOS transistor 22 is shown with its source coupled to the pin of circuit 10. Therefore, it would have been obvious to one of ordinary skill in the art to also believe the body connection of transistor 22 is coupled to the circuit's pin, thus rendering claims 20 and 21 obvious. Unless a reference clearly indicates otherwise, with respect to the

body connection (e.g. bulk, body, or backgate) of a MOS transistor is typically connected to the transistor's source. In this case, the body connection of transistor 22 is considered connected to its source, which is connected to the pin of circuit 10. For the same reasoning as applied to closely related claims 2, and 5-7 described within the 35 U.S.C. 102(b) rejections, claims 22, and 24-26 are also rendered obvious. Konishi discloses that 22 (within what is deemed the signal transfer circuit) provides a large current to help compensate for a decrease in VC2 (e.g. see column 2, lines 11-20). Since charge storage circuit 23 is charged to VC2, one of ordinary skill in the art can consider the signal transfer circuit of Konishi as being configured to prevent the stored charge from falling below a level required to power the pin of circuit 10, thus rendering obvious claim 23. Konishi discloses the operating voltage VC2 equals VR – VT (i.e. see column 1, line 66 through column 2, line 15).

No claim is allowable as presently written.

Allowable Subject Matter

However, Claims 8-13, and 27-31 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims, where applicable. There is presently no strong motivation to modify or combine any prior art reference to ensure the inverting circuit receives the first, second, and bias signals as recited within independent claims 8 and 27, upon which respective claims 9-13 and 28-31 depend.

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least some claimed limitations. Although not used in any formal rejections, Shin shows an apparatus in Fig. 3 comprising a charge storage circuit C2 receiving a first signal Vref provided

from a signal transfer circuit (e.g. all the other components shown), wherein one of ordinary skill in the art would know first signal could be used to power a circuit. Also, it would be obvious to one of ordinary skill in the art that when a transient event occurs (e.g. supply Vcc temporarily decreases as shown in Fig. 4), charge storage circuit would help maintain Vref by providing what can be deemed a second signal. Cho shows an apparatus in Fig. 3 comprising a signal transfer circuit 70, charge storage circuit 74, inverting circuit 80 (or 81,82), bias Vbias, and what one of ordinary skill in the art could deem the first/second signals (at D). However, the inverting circuit 80 (or 81,82) does not receive bias Vbias as recited within claims 8 and 27. Due to some of these circuit's similarities with the applicants' circuits and claimed limitations, the references should still be carefully reviewed and considered.

Response to Arguments

The applicants' arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. The prior art references cited in the present Office Action's rejections show/disclose circuitry that provides power to a circuit during normal operation, and during transient events. As described within the rejections, the circuitry comprises a signal transfer circuit that provides a first signal, and a charge storage circuit that provides a second signal during their respective periods of operation.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is

(703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE
Terry L. Englund

5 Jun 2003

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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